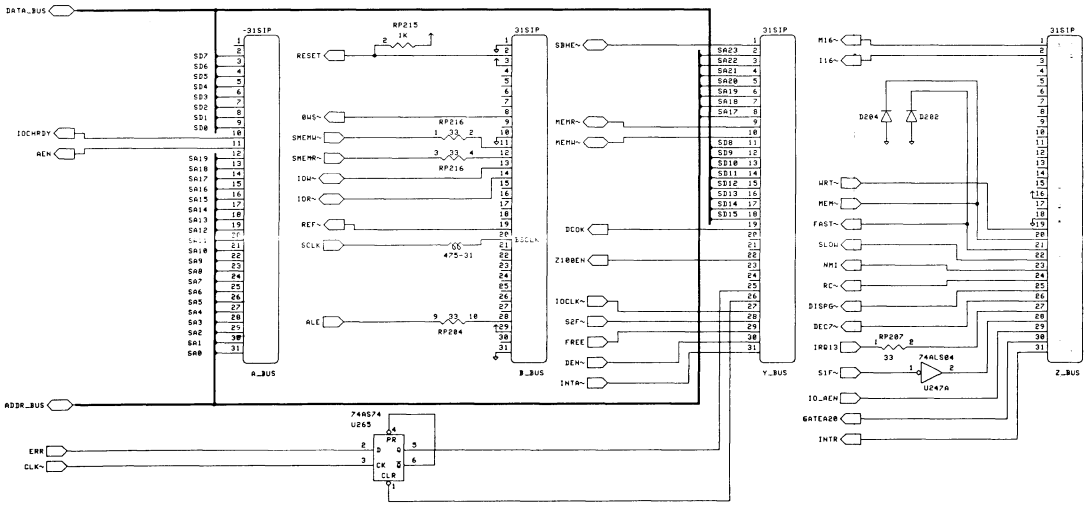
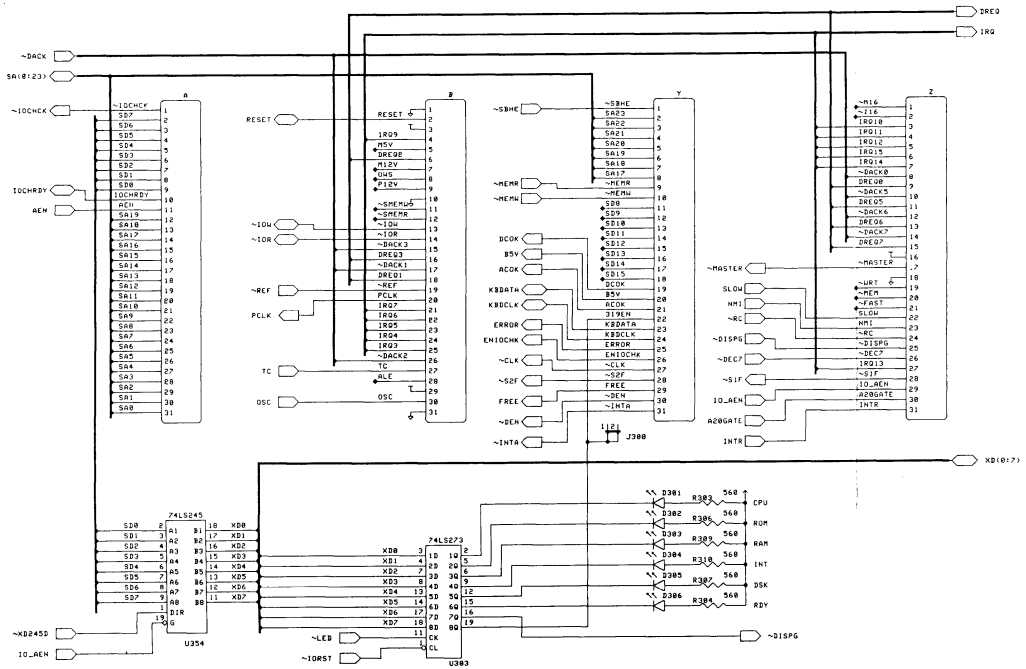


CPU/RAM Card



I/O Card

Figure A-1: Backplane Signal Interface Schematic

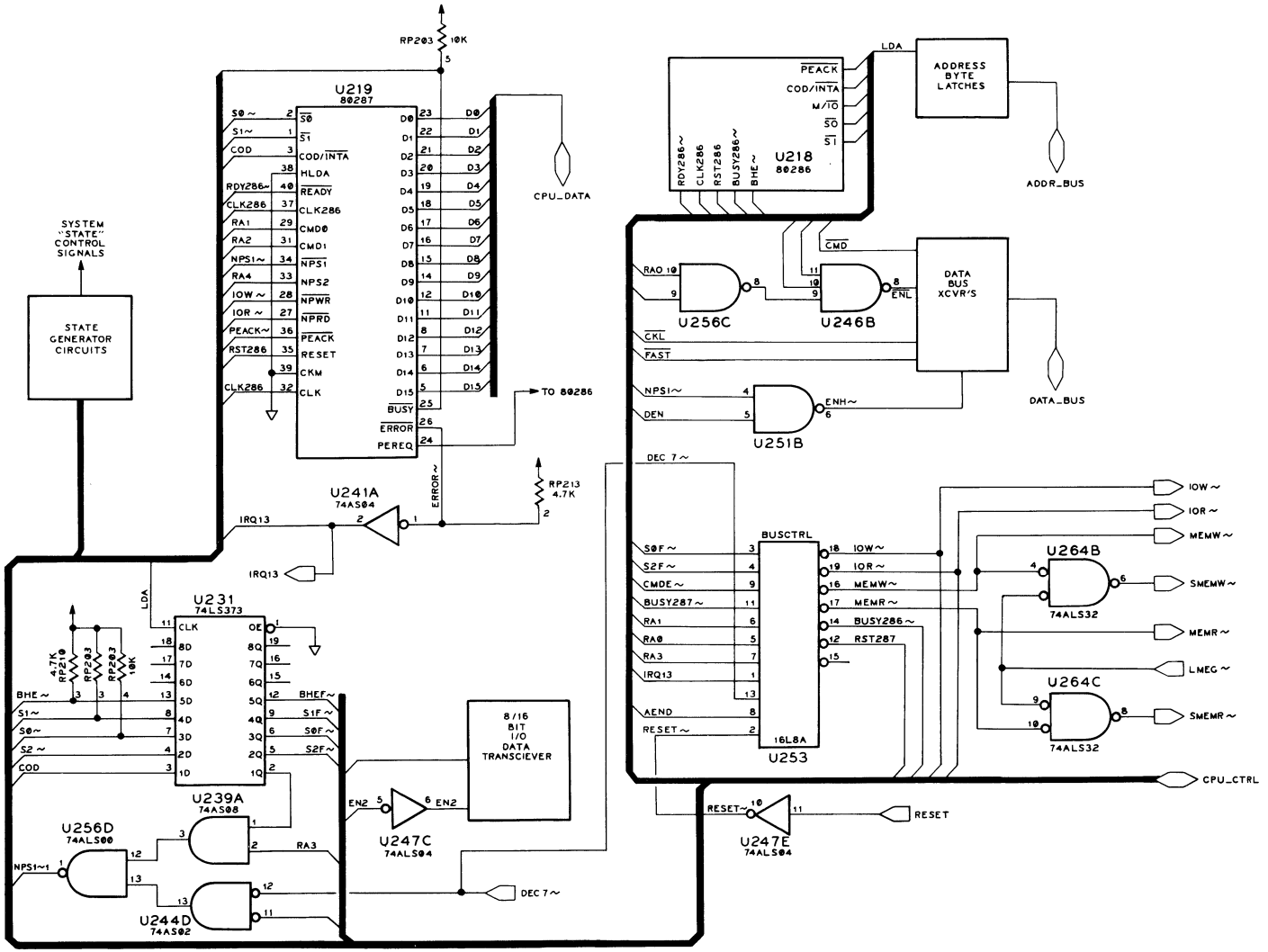


Figure A-2: Control Bus Schematic

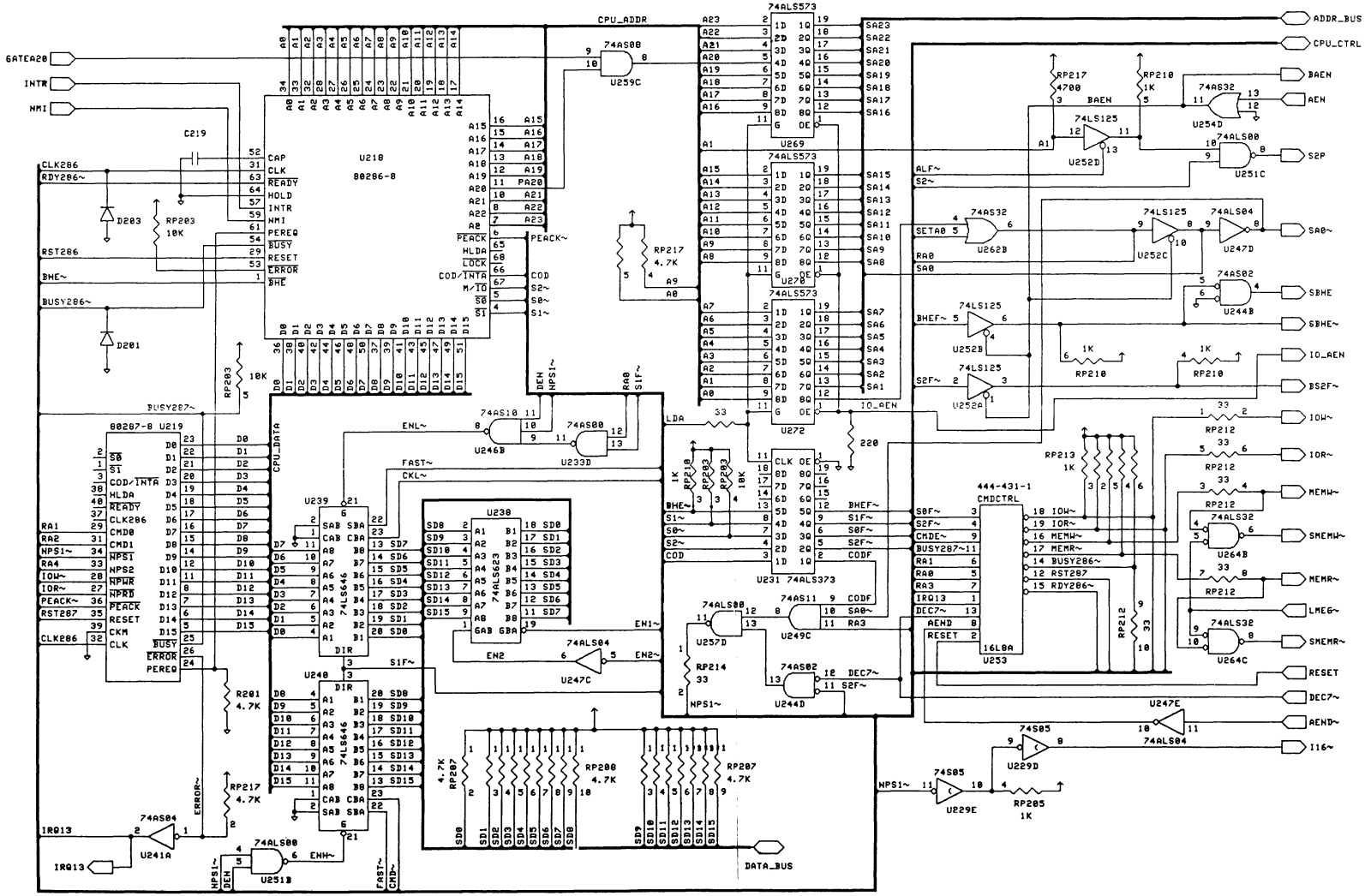


Figure A-3: CPU Control Logic Schematic, Part 1

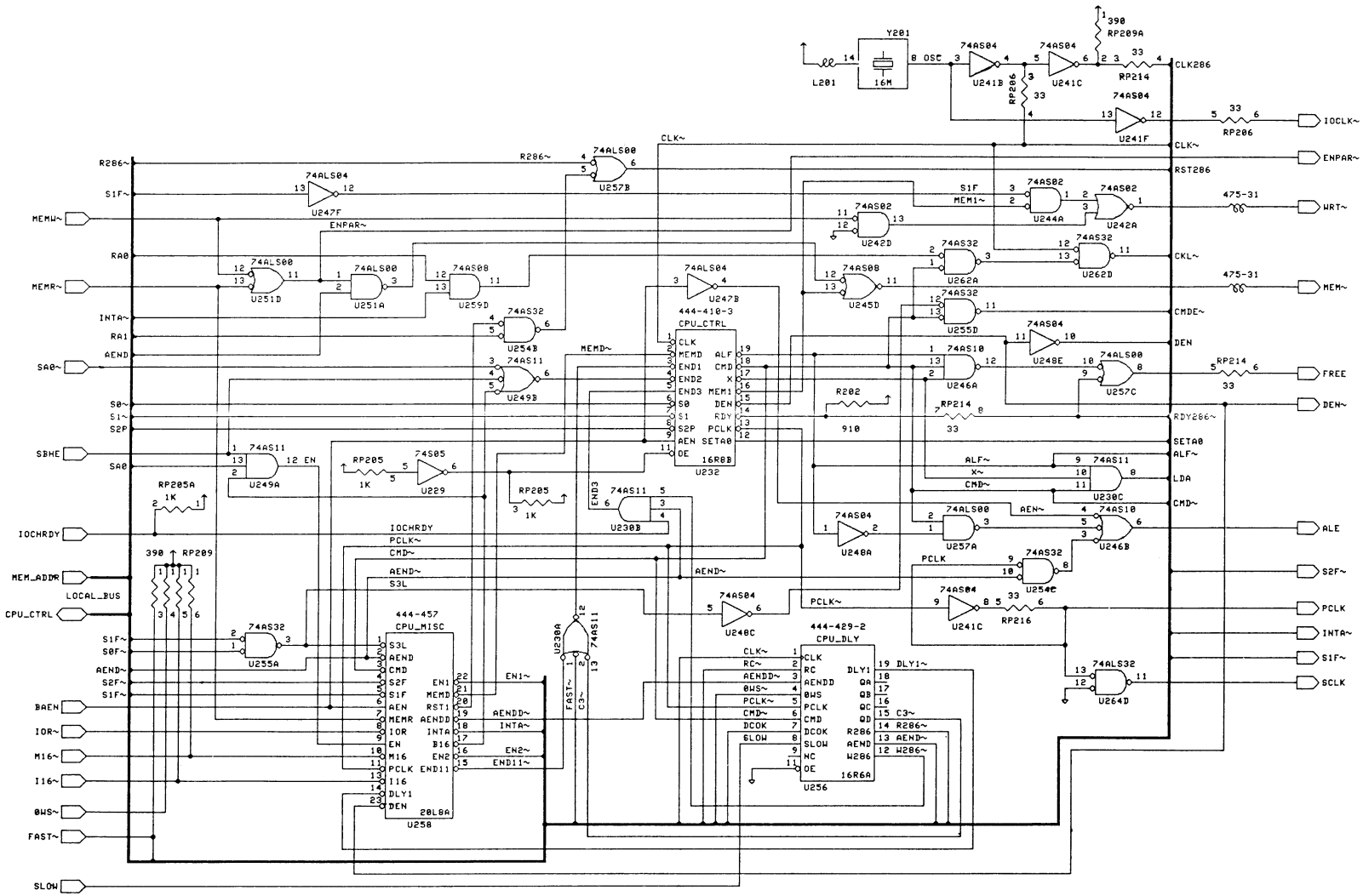


Figure A-4: CPU Control Logic Schematic, Part 2

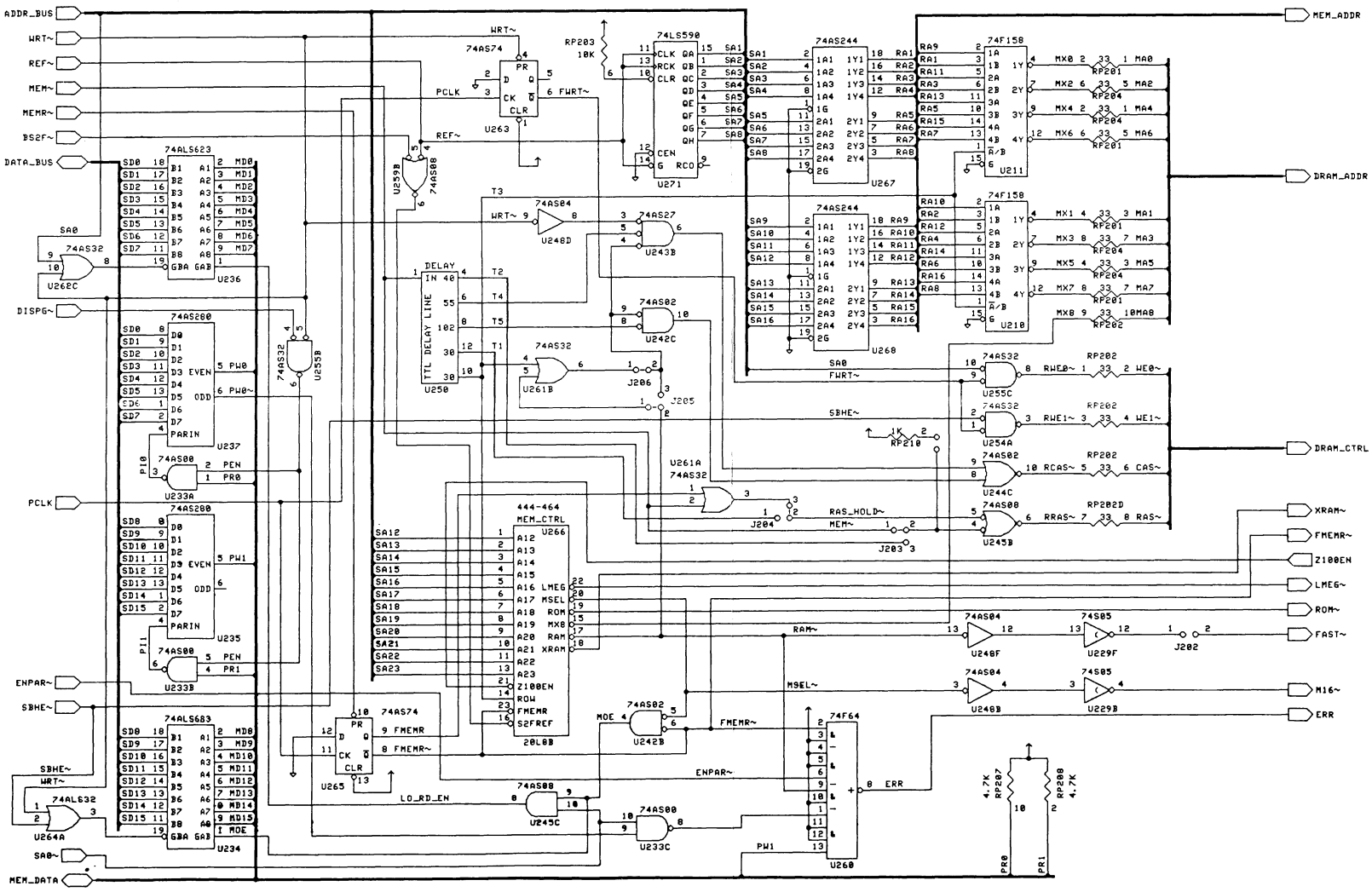


Figure A-5: Memory Control Logic Schematic

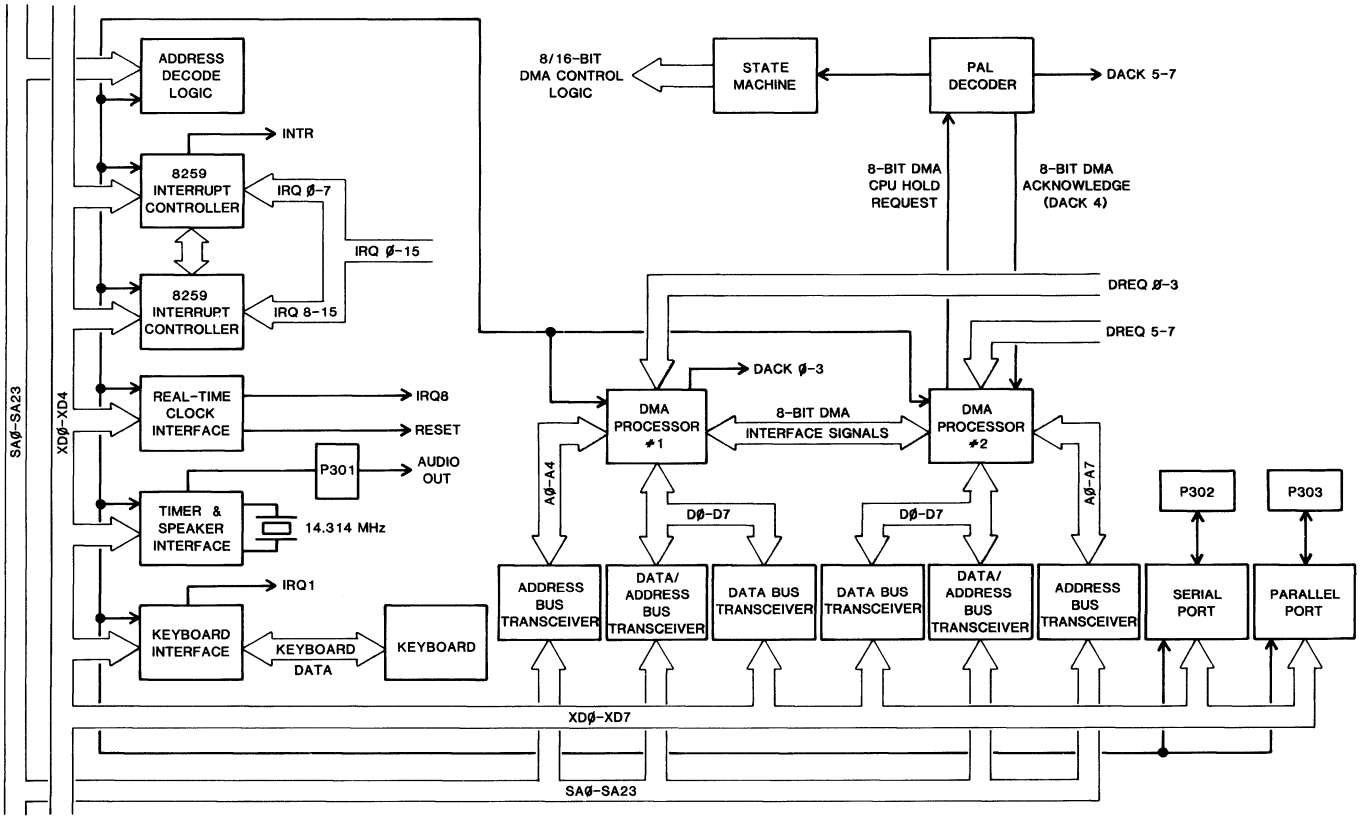


Figure A-6: I/O Card Block Diagram

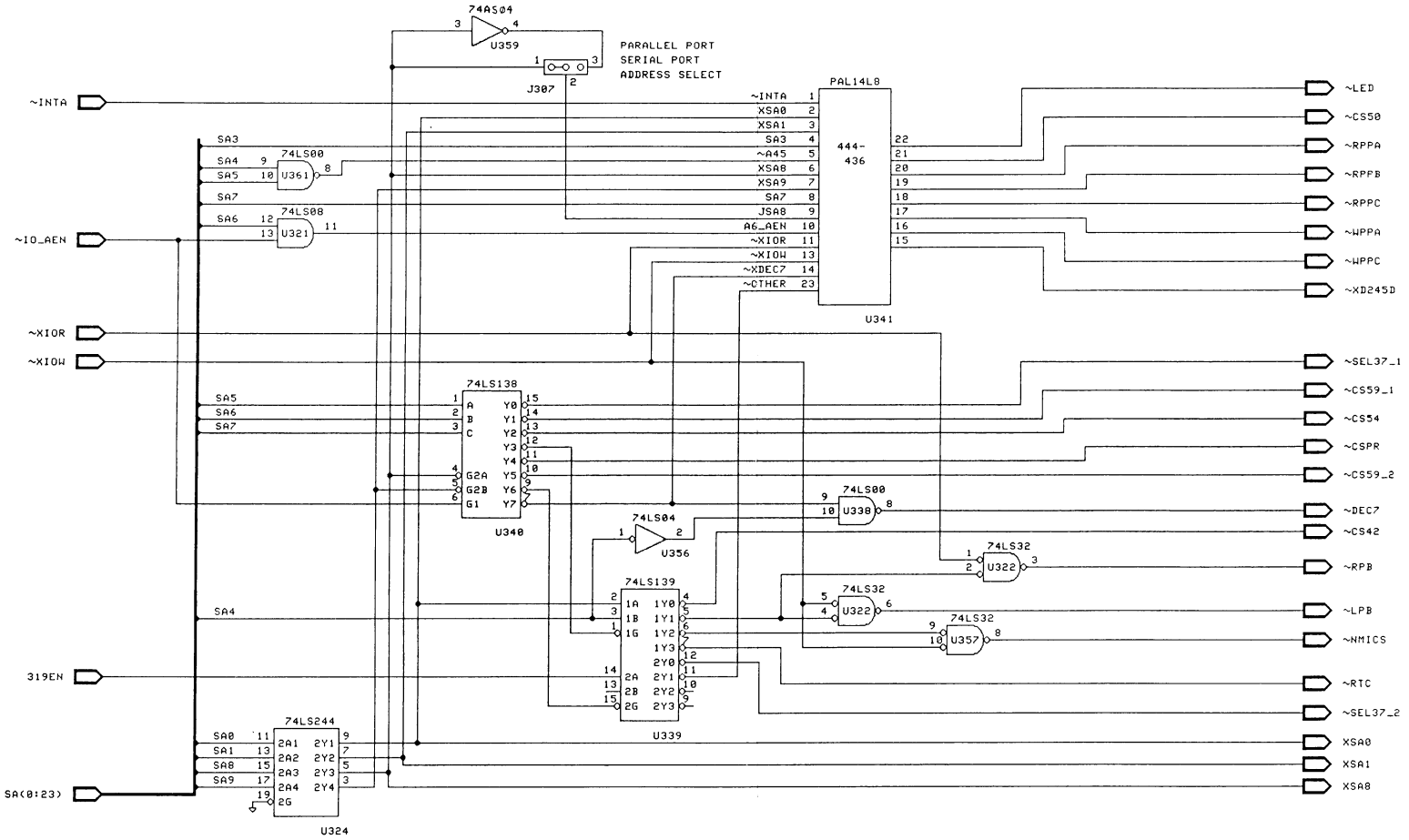


Figure A-7: Address Decode Logic Schematic

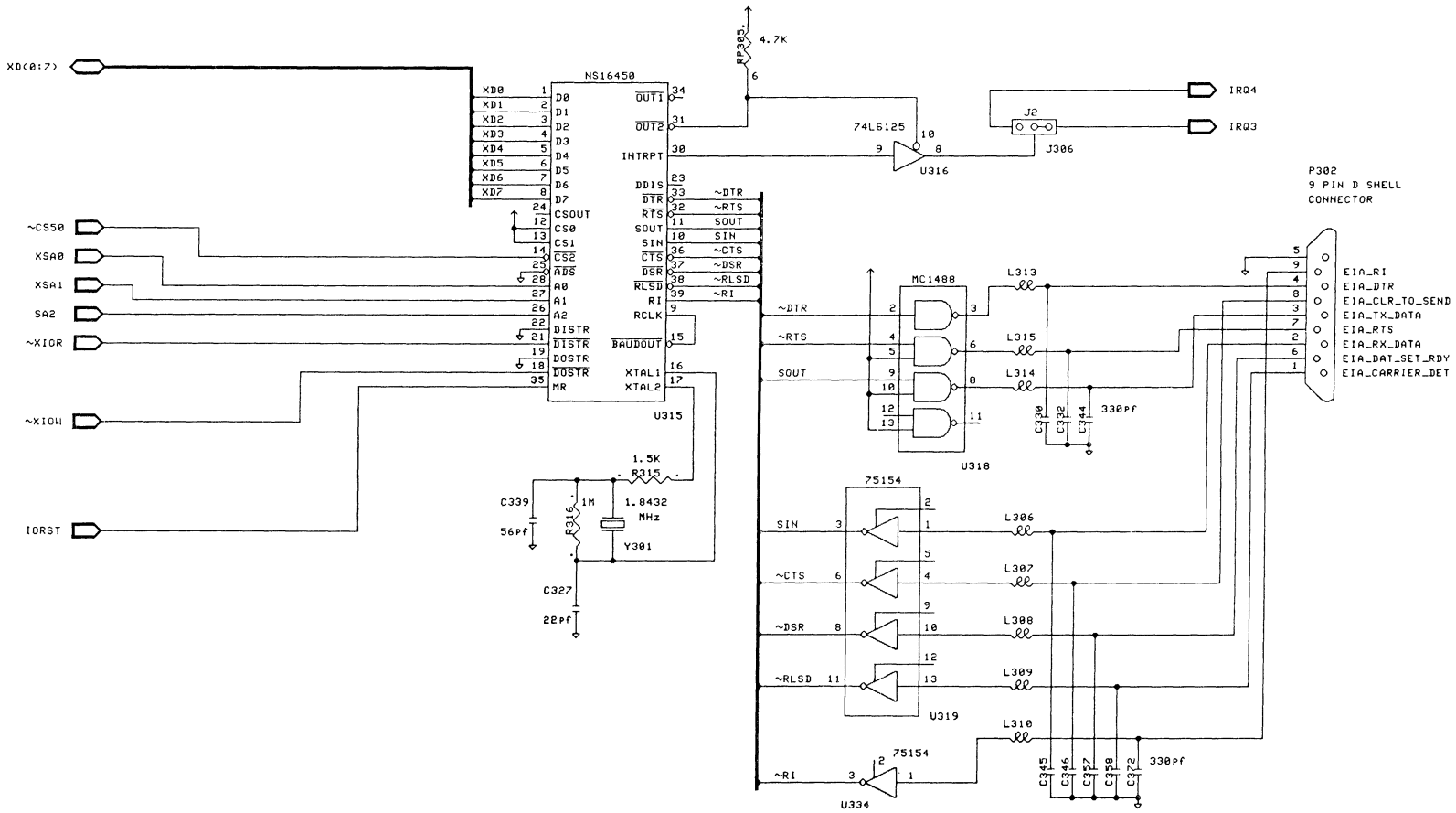


Figure A-8: Serial Port Schematic

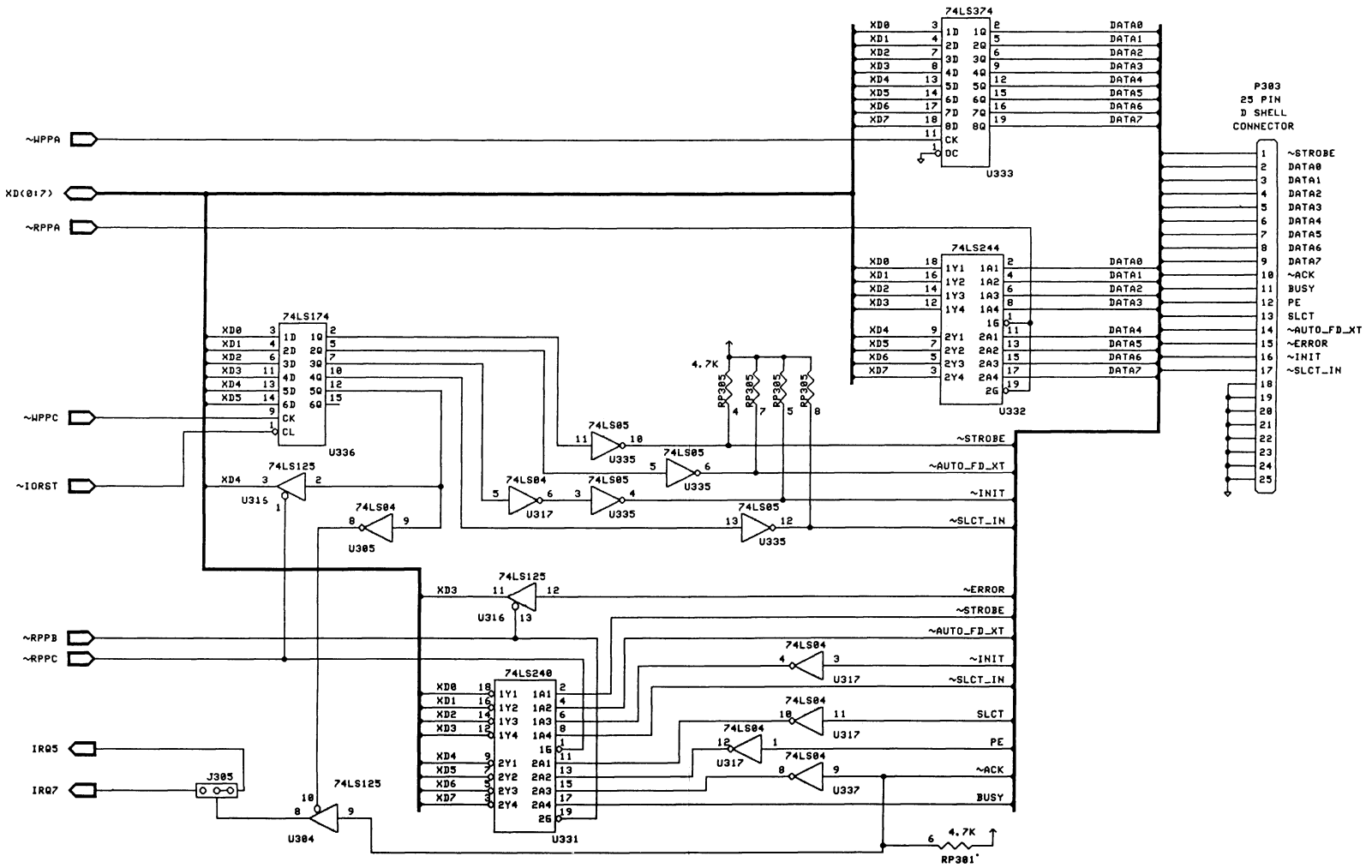


Figure A-9: Parallel Port Schematic

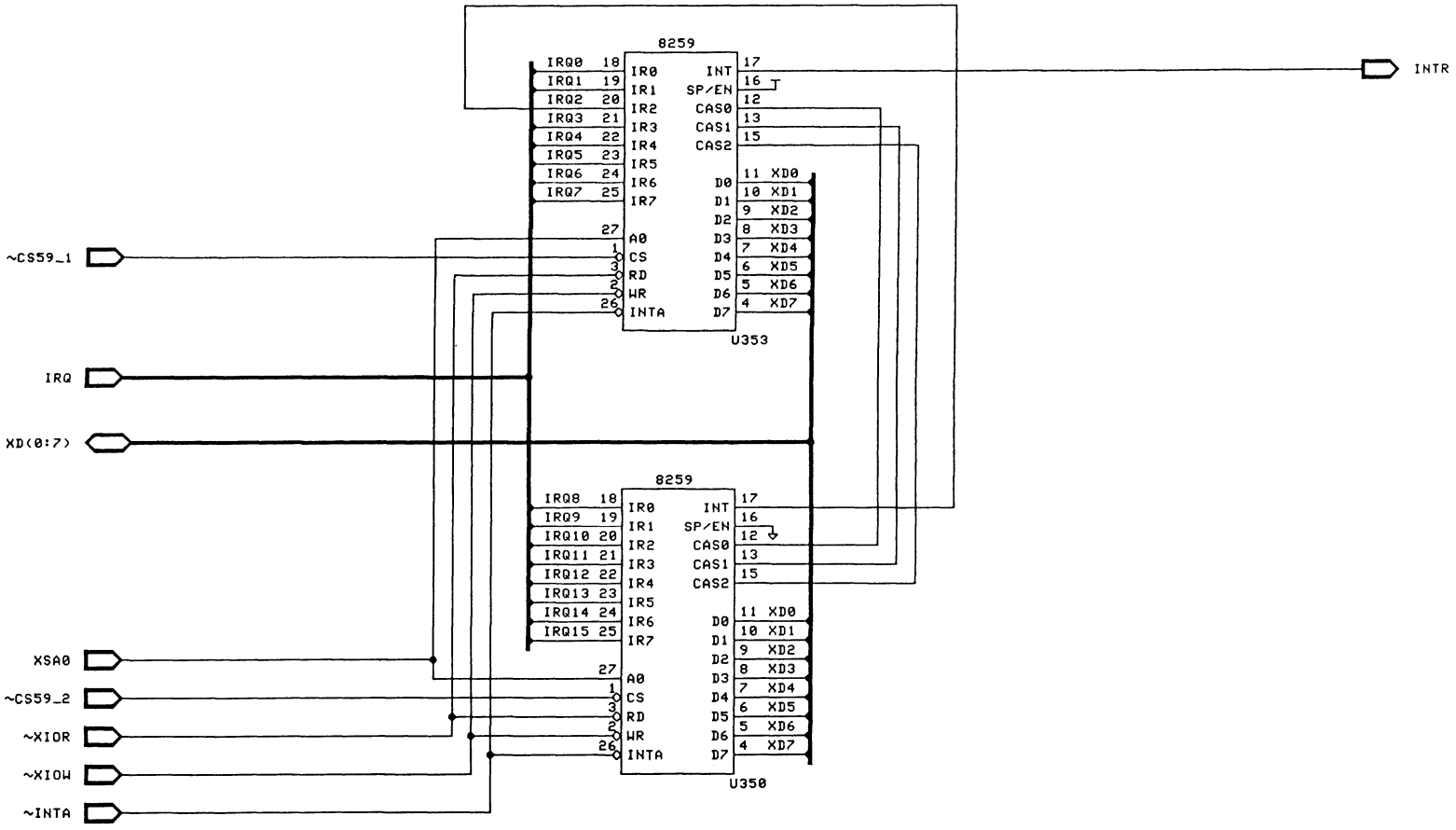


Figure A-10: Interrupt Control Schematic

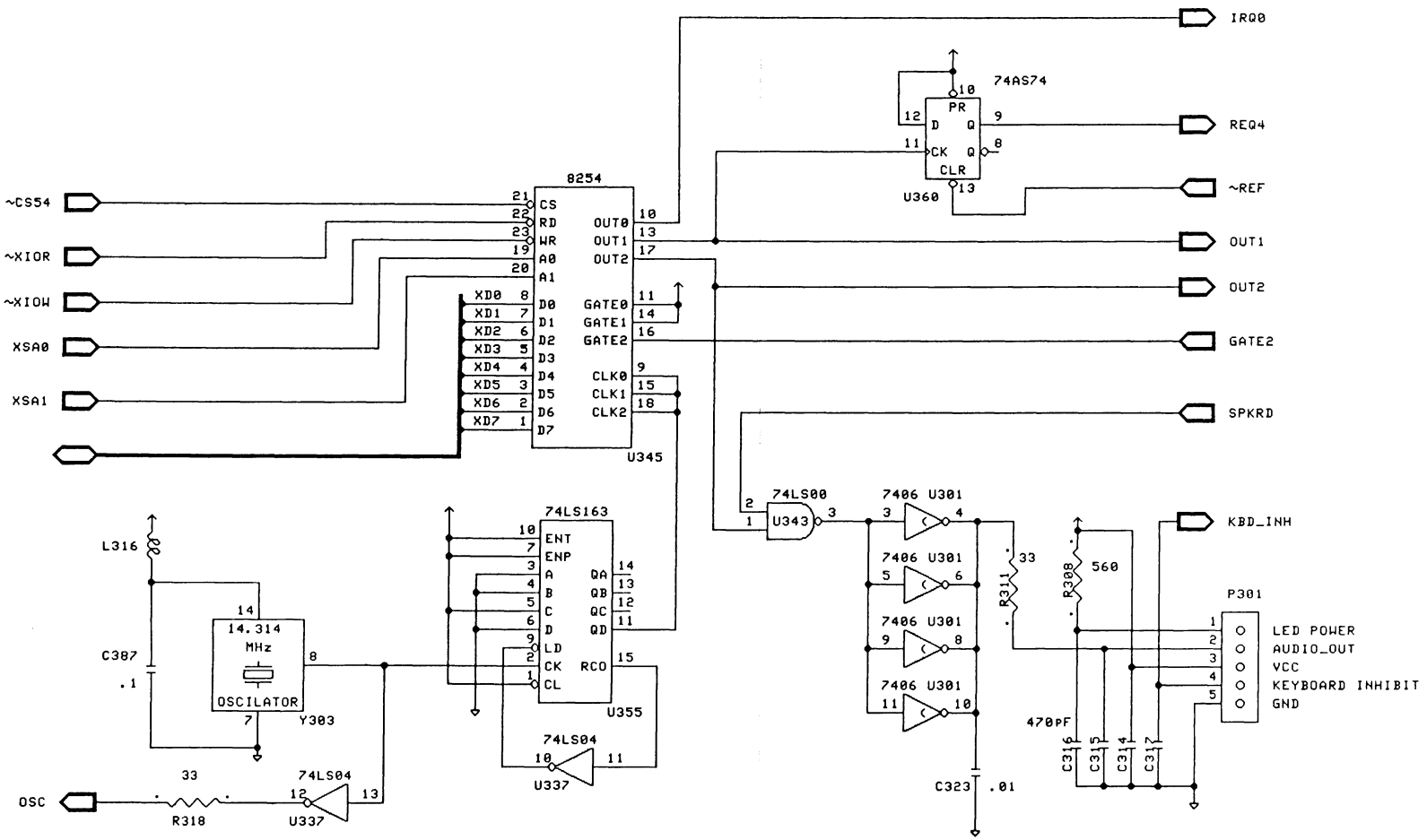


Figure A-11: Programmable Interval Timer Schematic

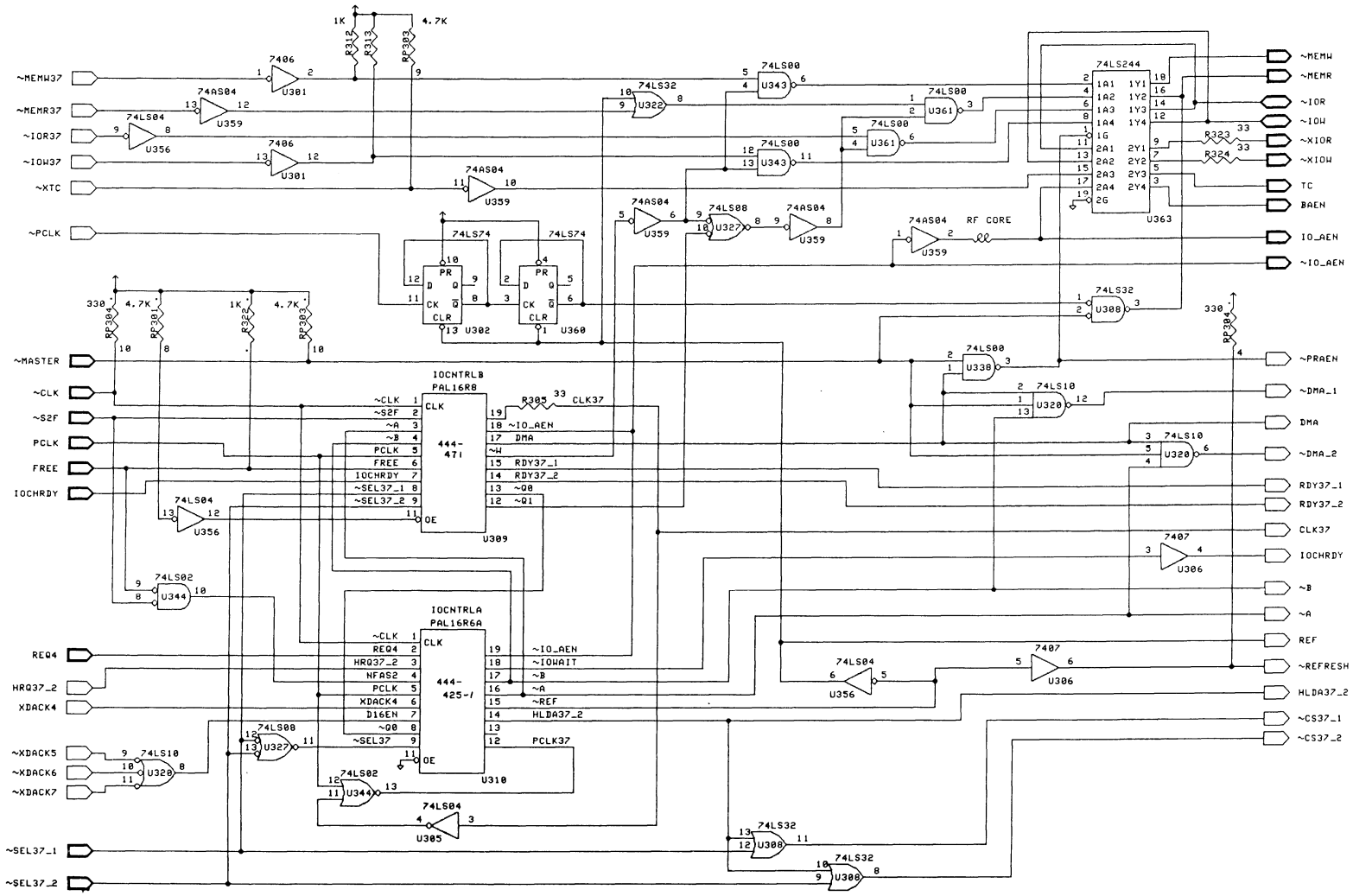


Figure A-12: DMA Control Schematic, Part 1

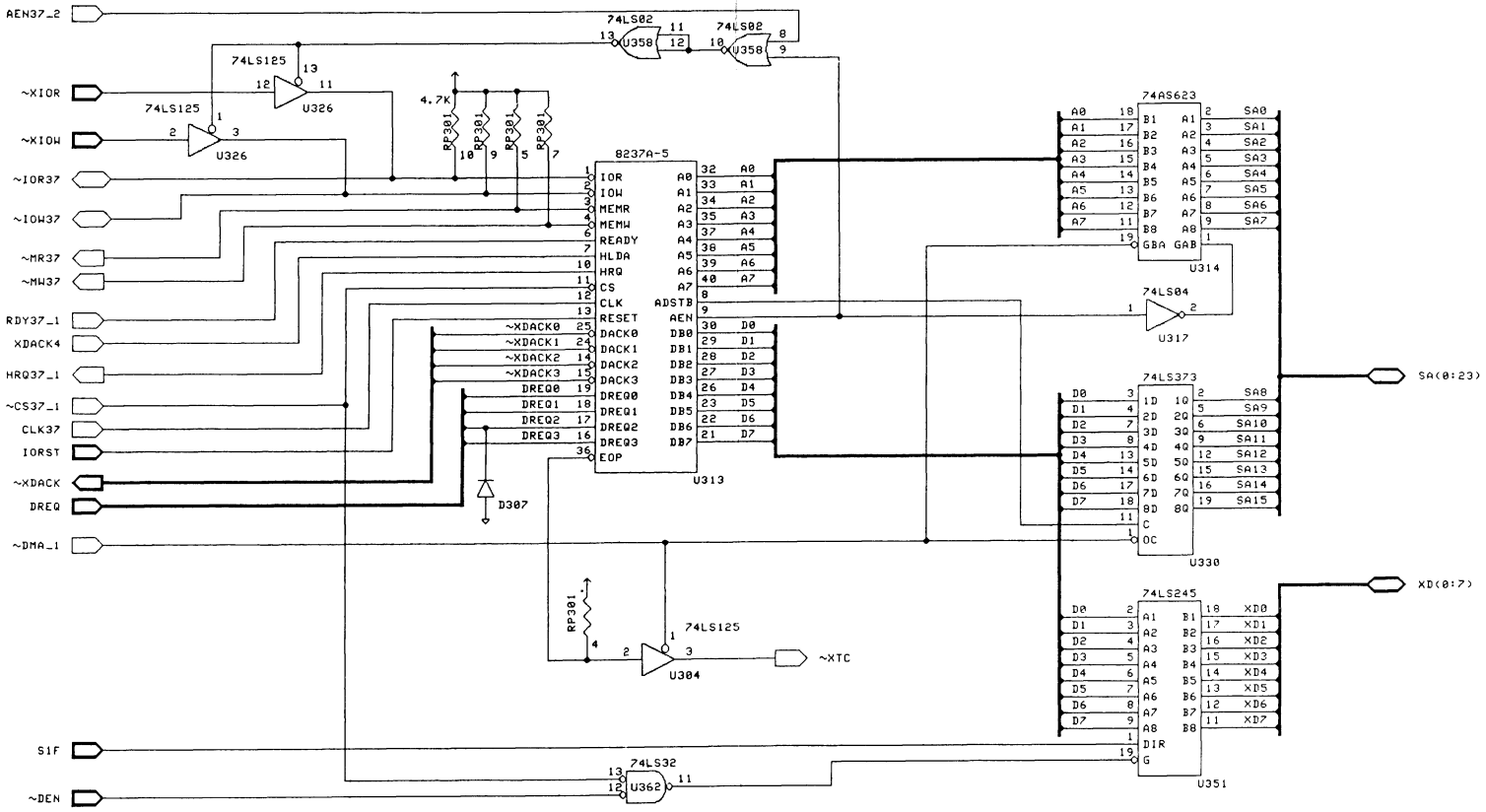


Figure A-13: DMA Control Schematic, Part 2

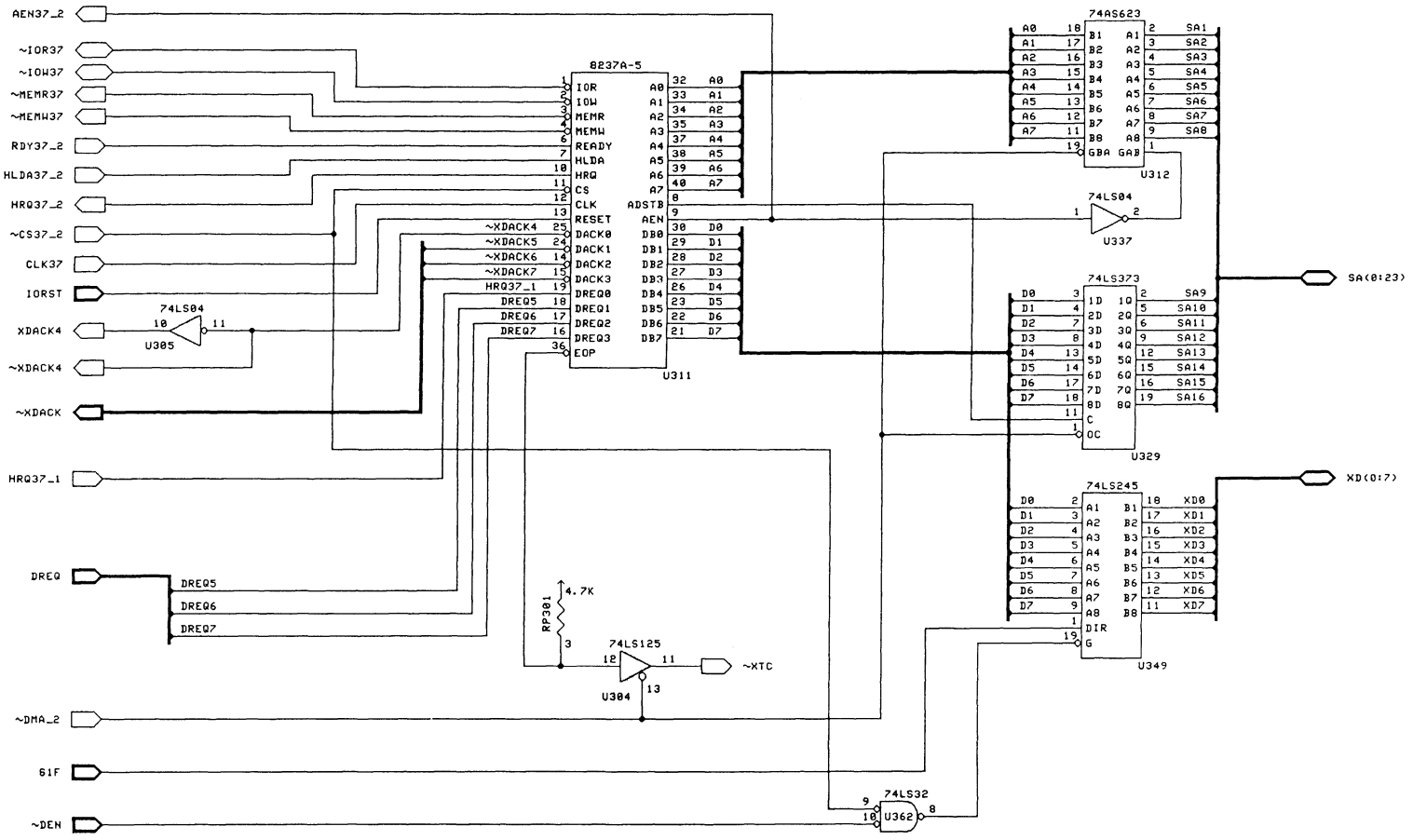


Figure A-14: DMA Control Schematic, Part 3

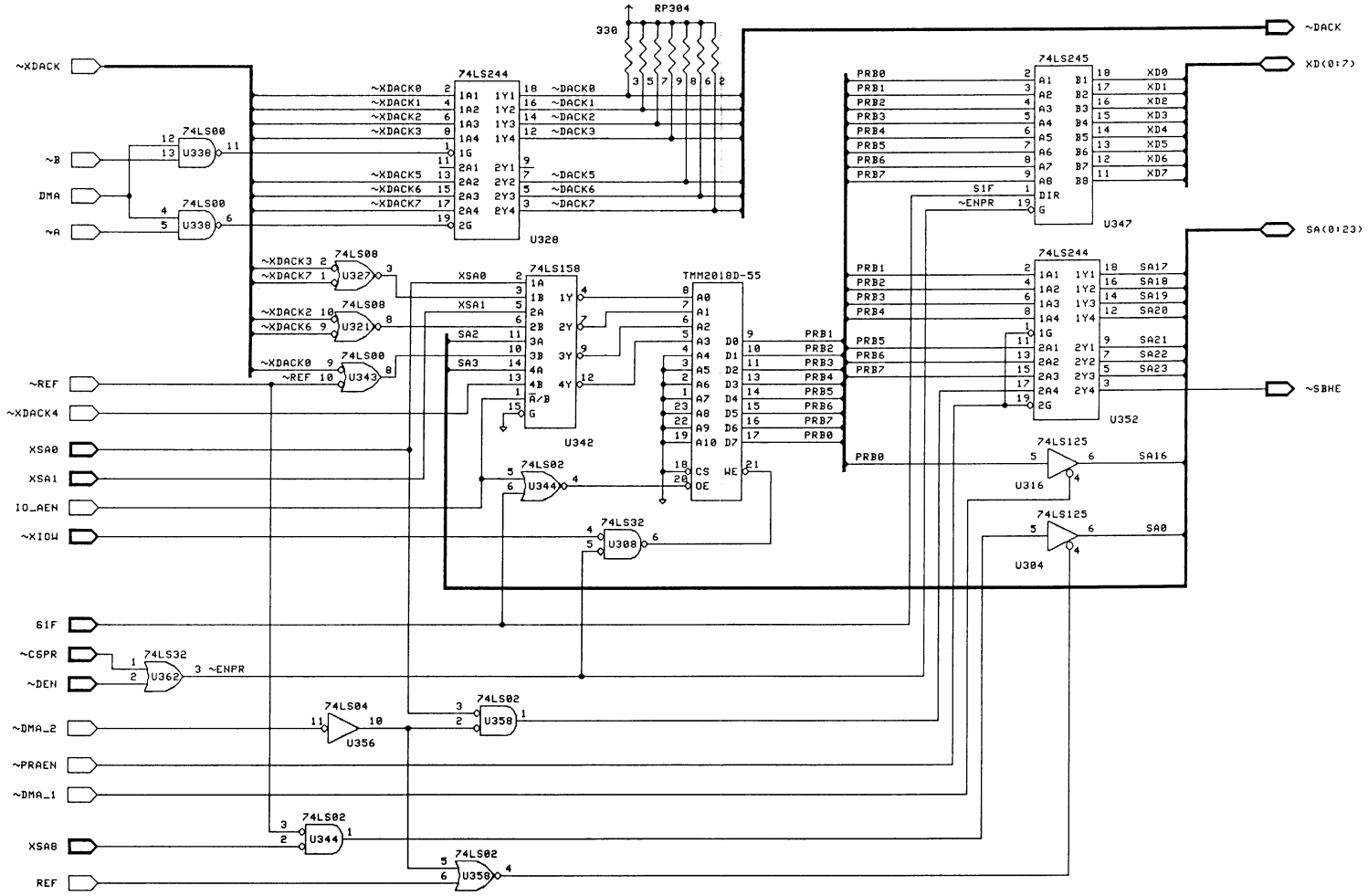


Figure A-15: DMA Control Schematic, Part 4

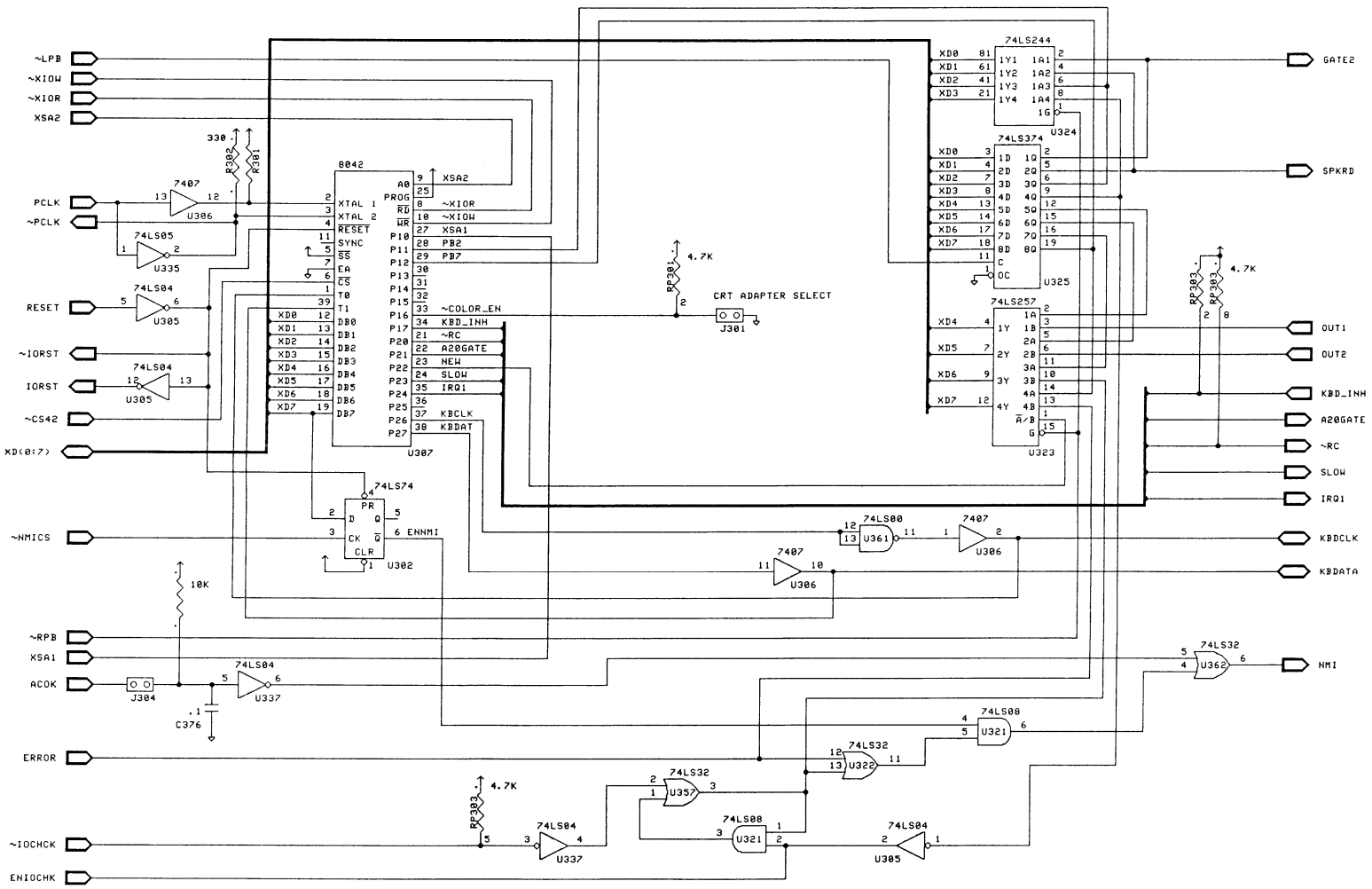


Figure A-16: Keyboard Interface Schematic

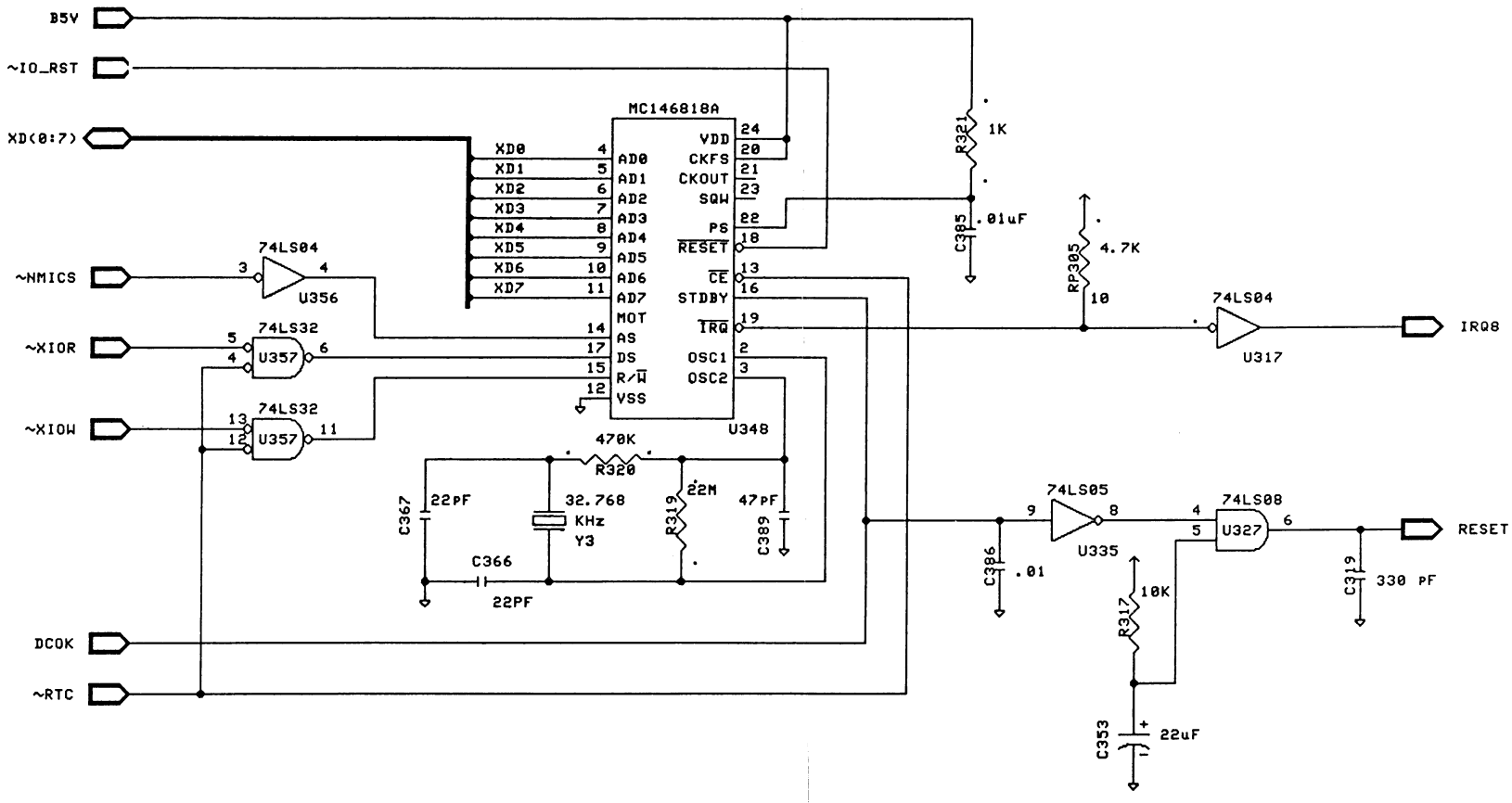


Figure A-17: Real-Time Clock Interface Schematic

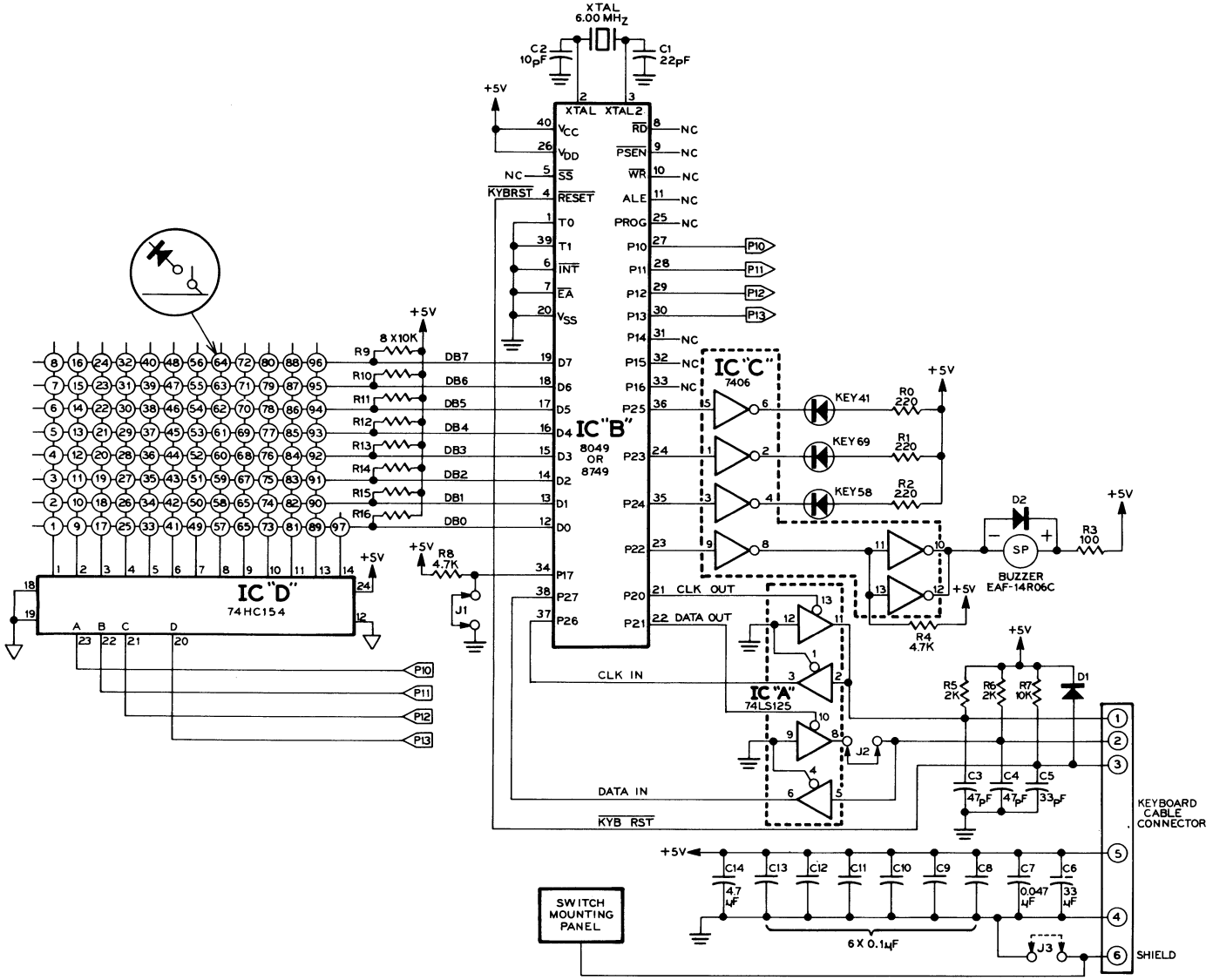


Figure A-18: Keyboard Schematic